Amendments to the Claims

1 - 2 (canceled)

3. (currently amended) ~~The~~ A reference signal generator ~~of claim 2~~, comprising:

an oscillator that provides an oscillator signal;

a buffer amplifier having an adjustable amplifier gain and coupled to process said oscillator signal into a reference signal that has a reference amplitude; and

a controller that adjusts said amplifier gain in response to said reference amplitude;

wherein said amplifier gain corresponds to a gain control signal and said controller includes:

at least one comparator that responds to said reference signal and provides a pulse train when said reference amplitude exceeds a predetermined threshold signal; and

in response to said pulse train, a counter that provides said gain control signal to thereby reduce said amplifier gain until said reference amplitude no longer exceeds said threshold signal;

and wherein said controller further includes:

a generator that responds to a first clock signal to provide a second clock signal, an enable signal and a subsequent disable signal;

a first gate that passes said second clock signal in response to said enable signal and blocks said second clock signal in response to said disable signal; and

a second gate that passes said second clock signal from said first gate to said counter in response to said pulse train.

4. (currently amended) The generator of claim 3 [[2]], wherein said comparator is a differential pair of transistors.

5. (currently amended) The generator of claim 3 [[2]], wherein said buffer amplifier includes:

at least one set of current generators that provide a current with a current amplitude that corresponds to said gain control signal; and

an inverter that carries said current to provide said reference signal with said reference amplitude thereby corresponding to said gain control signal.

6. (previously presented) The generator of claim 5, wherein said current generators are configured with binarily-related currents so that said current amplitude has a binary relationship to said gain control signal.

7. (canceled)

8. (currently amended) The generator of claim 9 [[1]], wherein said buffer amplifier includes:

a plurality of resistors; and

a plurality of switches that selectively access said resistors in response to said controller to thereby adjust said amplifier gain.

9. (currently amended) ~~The~~ A reference signal generator ~~of claim 2~~, comprising:

an oscillator that provides an oscillator signal;

a buffer amplifier having an adjustable amplifier gain and coupled to process said oscillator signal into a reference signal that has a reference amplitude; and

a controller that adjusts said amplifier gain in response to said reference amplitude;

wherein said amplifier gain corresponds to a gain control signal and said controller includes:

at least one comparator that responds to said reference signal and provides a pulse train when said reference amplitude exceeds a predetermined threshold signal; and

in response to said pulse train, a counter that provides said gain control signal to thereby reduce said amplifier gain until said reference amplitude no longer exceeds said threshold signal;

and wherein said at least one comparator comprises upper and lower comparators that respectively respond to upper and lower predetermined threshold signals.

10. (currently amended) The generator of claim 9 [[1]], wherein said oscillator is a digitally-controlled crystal oscillator.

11. (canceled)

12. (currently amended) The generator of claim 15 ~~11~~, wherein said buffer amplifier includes a plurality of current generators that are responsive to said gain control signal.

13. (previously presented) The generator of claim 12, wherein each of said current generators includes:

a plurality of resistors; and

a plurality of switches that selectively access said resistors in response to said gain control signal to thereby adjust said amplifier gain.

14. (previously presented) The generator of claim 12, wherein said buffer amplifier provides said reference signal at a reference port and each of said current generators includes:

a plurality of resistors;

a plurality of access switches that access selected ones of said resistors in response to said controller; and

an output switch that couples selected resistors to said reference port in response to said oscillator signal.

15. (currently amended) ~~The~~ A reference signal generator ~~of claim 16~~, comprising:

an oscillator that provides an oscillator signal;

a buffer amplifier having an amplifier gain that corresponds to a gain control signal and coupled to process said oscillator signal into a reference signal that has a reference amplitude; and

a controller that adjusts said gain control signal in response to said reference amplitude;

wherein said controller includes:

a counter that counts a clock signal to thereby generate said gain control signal; and

a comparator that provides said clock signal to said counter in response to a comparison of said reference signal and a threshold signal;

wherein said controller further includes:

a string of resistors coupled to provide selectable voltages; and

a plurality of transistors coupled to selectively provide one of said voltages as said threshold signal;

and wherein said controller further includes a differential pair of amplifiers that transfers a common mode level of said reference signal to said string of resistors.

16. (canceled)

17. (currently amended) The generator of claim 15 ~~18~~, wherein said comparator comprises a differential pair of transistors.

18. (canceled)

19. (currently amended) ~~The~~ A reference signal generator ~~of claim 16~~, comprising:

an oscillator that provides an oscillator signal;

a buffer amplifier having an amplifier gain that corresponds to a gain control signal and coupled to process said oscillator signal into a reference signal that has a reference amplitude; and

a controller that adjusts said gain control signal in response to said reference amplitude;

wherein said controller includes:

a counter that counts a clock signal to thereby generate said gain control signal; and

a comparator that provides said clock signal to said counter in response to a comparison of said reference signal and a threshold signal;

and wherein said controller further includes a gate inserted to pass said clock signal to said counter in response to said comparator.

20. (previously presented) The generator of claim 19, wherein
said comparator generates a pulse train when said reference signal exceeds said threshold signal; and
said gate passes said clock signal in response to said pulse train.

21. (previously presented) The generator of claim 20, wherein said controller further includes a generator that provides an enable signal to enable said gate and a subsequent disable signal to disable said gate.

22. (currently amended) ~~The~~ A reference signal generator ~~of claim 11~~, comprising:
an oscillator that provides an oscillator signal;
a buffer amplifier having an amplifier gain that corresponds to a gain control signal and coupled to process said oscillator signal into a reference signal that has a reference amplitude; and
a controller that adjusts said gain control signal in response to said reference amplitude;
wherein said controller includes:
a counter that counts a clock signal to thereby generate said gain control signal;
upper and lower comparators that generate pulse trains when said reference signal exceeds predetermined threshold signals; and
a gate that passes said clock signal to said counter in response to said pulse trains.

23. (previously presented) The generator of claim 22, wherein said controller further includes:
a differential pair of amplifiers that provides a common mode level of said reference signal; and
a string of resistors that provides said threshold signals in response to said common mode level.

24. (previously presented) The generator of claim 22, wherein said controller further includes a generator that provides an enable signal to enable said gate and a subsequent disable signal to disable said gate.

25. (currently amended) The generator of claim 22 ~~11~~, wherein said oscillator is a digitally-controlled crystal oscillator.

26. (canceled)

27. (currently amended) ~~The~~ A synthesizer ~~of claim 29~~, comprising:
a voltage-controlled oscillator;
a phase detector that provides a control signal to said voltage-controlled oscillator;
a first frequency divider coupled between said voltage-controlled oscillator and said phase detector;
a reference oscillator that generates an oscillator signal;
a second frequency divider coupled between said reference oscillator and said phase detector;
a buffer amplifier having an adjustable amplifier gain and coupled to process said oscillator signal into a reference signal that has a reference amplitude; and
a controller that adjusts said amplifier gain in response to said reference amplitude;
wherein said controller includes:
a counter set to an initial count that maximizes said amplifier gain and coupled to provide a subsequent count of a clock signal that reduces said amplifier gain; and
a comparator that terminates said subsequent count when said reference amplitude reaches a threshold amplitude;
and wherein said controller further includes:
a gate coupled to pass said clock signal to said counter; and
a generator that provides an enable signal to enable said gate and a subsequent disable signal to disable said gate.

28. (currently amended) The synthesizer of claim 27 ~~29~~, wherein said controller further includes:
a differential pair of transistors that provide a common mode level of said reference signal; and
a resistor string that provides said threshold amplitude in response to said

common mode level.

29. (canceled)

30. (currently amended) The synthesizer of claim 27 ~~26~~, wherein said buffer amplifier includes:

a plurality of resistors; and

a plurality of switches that selectively access said resistors in response to said controller to thereby adjust said amplifier gain.

31. (new) A reference signal generator, comprising:

an oscillator that provides an oscillator signal;

a buffer amplifier having an amplifier gain that corresponds to a gain-control signal and arranged to amplify the amplitude of said oscillator signal to thereby provide a reference signal;

a low-pass filter which extracts a common-mode level from said reference signal;

a string of resistors which defines upper and lower tap points and a junction between said upper and lower tap points;

an input differential pair of transistors having an output coupled to drive said string and having a differential input coupled between said filter and said junction to thereby transfer said common-mode level to said junction;

an upper differential pair of transistors that generates a first pulse train in response to its differential input which is coupled between said reference signal and a selected one of said upper tap points;

a lower differential pair that generates a second pulse train in response to its differential input which is coupled between said reference signal and a selected one of said lower tap points; and

a counter that is enabled by said first and second pulse trains to count a clock signal to thereby generate a count which comprises said gain-control signal;

wherein increase of said count decreases said amplifier gain until said first and second pulse trains cease.

32. (new) The generator of claim 31, wherein said buffer amplifier includes:
upper and lower sets of resistors;
an inverter coupled between said upper and lower sets and having an input coupled to receive said oscillator signal from said oscillator and an output which provides said reference signal; and
upper and lower transistor switches respectively arranged to selectively couple resistors of said upper and lower sets to a power supply in response to said gain-control signal.

33. (new) The generator of claim 32, wherein the resistances of the resistors of said sets are binarily related.

34. (new) The generator of claim 31, further including:
a first set of tap transistors that are each inserted between a respective one of said upper tap points and said upper differential pair to selectably provide said selected upper tap point; and
a second set of tap transistors that are each inserted between a respective one of said lower tap points and said lower differential pair to selectably provide said selected lower tap point.

35. (new) The generator of claim 31, further including:
a gate that passes said clock signal to said counter in response to presence of said first and second pulse trains; and
a clock generator arranged to provide said clock signal for a time sufficient to accommodate a decrease of said amplifier gain.